An Alignment Insensitive Separable Electromagnetic Coupler for High-Speed Digital Multidrop Bus Applications

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***Abstract*—A separable electromagnetic coupler was designed, simulated, fabricated, and tested as part of a prototype eight-module multidrop memory bus. The coupler consists of broadside coupled traces, one on a rigid motherboard and the other on a flex circuit soldered to a daughter card. The zig–zag geometry of the traces reduces variation in the coupling coefficient due to horizontal and vertical misalignment of the coupler halves. Simulation and testing indicates that a target capacitive coupling coefficient of 0.34, which has been selected to balance signal-transmission-level requirements against motherboard impedance discontinuity effects, can be achieved with little variation over +/−12-mil alignment tolerance. In addition, custom interface circuitry was designed in conjunction with the coupler to enable 1.6-Gb/s data rate per differential pair. The prototype system was tested for an extended period executing read and write memory transactions for an estimated bit error rate less than 2.0e-17.**

***Index Terms*—Bus transfers, connectors, coupled transmission lines, high-speed integrated circuits.**

I. Introduction

PREVIOUS attempts to reach high data rates on multidrop buses have had difficulty due to the signal integrity problems created by transmission-line stubs. The T-junction formed by these stubs with a motherboard transmission line creates an inherent impedance discontinuity. Moreover, parasitic capacitances and inductances due to the typically employed connectors create their own reflections. These reflections produce inter-symbol interference (ISI) and degrade the reliability of the channel in terms of bit error rate (BER). An alternative approach is to replace these stub connections with directional couplers. Earlier examples of this coupled approach to multiload bus networks can be found in the work of Bolt and Nick [1], De Veer and Nick [2], and more recently, Osaka *et al.* [3].

Fig. 1 shows a system-level block diagram of the prototype memory system and highlights the use of ac coupling [4], [5] for distributing memory commands, address, data, and clocks to the memory modules. A single coupler replaces each direct connection on a stub-based multidrop bus. As shown in Fig. 1, each module contains a buffer chip, which translates the coupled signals to standard logic levels for the commodity dynamic random access memory chips (DRAMs). A memory controller communicates with up to eight cards on a multidrop bus. All signaling is differential in contrast to earlier approaches [1]–[3], and signals are parallel terminated at both ends on the motherboard and cards (discrete resistors at far ends, calibrated on-chip transistor termination at near ends). The ac transmission-line coupling, targeted in a light coupling range, minimizes ISI by maintaining impedance continuity along the bus and isolating the bus from on-card parasitics. The coupling range meets a dual constraint: not too large for ISI (e.g., reflection coefficients from -0.15 to -0.18 at coupled-to-uncoupled interfaces along the bus), while maintaining sufficient pulse height and pulsewidth at the receiver to ensure reliable data communication. Since the transmitted signals have effectively been differentiated by the high-pass characteristics of the coupling, receiver circuits are designed to "invert" this transfer function before the data can be recovered. Note that the ac coupling is bilaterally symmetric so the signals and I/O circuits in both directions are the same.

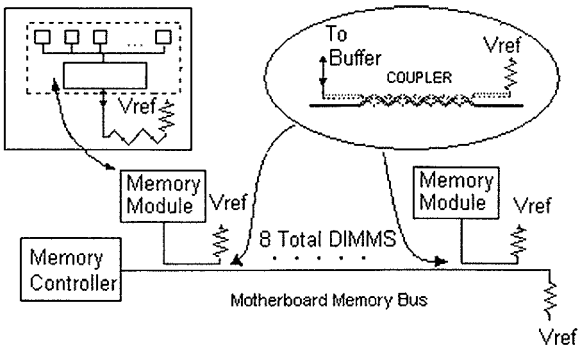

Fig. 1. Memory bus block diagram.

In Section II, we describe the electrical considerations in the coupler design and relate them to near-and far-end crosstalk coefficients. Section III describes the mechanical design of a separable coupler using conventional low-cost materials. Simulation and modeling of the coupler is discussed in Section IV. Receiver circuit design is described in Section V. Section VI describes measurements and test results from coupler prototypes and the prototype eight-load memory system. Results are summarized in Section VII.

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II. Coupler Electrical Design

The signal integrity benefits of achieving a selected range of coupling performance can be illustrated by considering the simplest case of a lossless coupler embedded in a homogeneous dielectric, and where the propagation is essentially TEM. The amplitude of the coupled signal is determined by the capacitive and inductive coupling coefficients K_c and K_l, respectively. K_c is the ratio of the per unit length mutual capacitance between two conductors to the geometric mean of their per unit length self-capacitances. K_l is defined similarly for the conductor inductances. For this idealized case, the relationship between K_c and the reflection coefficient at the coupler can then be readily deduced, as well as the corresponding relationship between K_c and the transmission coefficient (transmission loss) to the last coupler [5]. From this simplified analysis, it is shown that the selected K_c range $(0.2 < K_c < 0.34)$ results in a worst case reflection coefficient range of 0.15–0.18, and that the corresponding signal transmission coefficient (signal attenuation) at the eighth coupler on the bus line is 0.3–0.4. In reality, adjustment of the differential transmission-line geometry in the feed and inter-coupler regions can be used to further minimize the impedance discontinuities resulting from the presence of the couplers on the transmission bus.

Traditional microwave couplers have been implemented on a single substrate so that the geometry of the coupling structure can be controlled to the tolerances of lithographic and etch processes. For a digital communications application, like a high data rate memory bus, it is often a requirement that the system be configured by an end user after manufacture. To utilize electromagnetic coupling in this context, it is necessary to develop a separable coupler where the two coupled conductors can be manufactured separately and then brought together as the system is constructed. The accuracy of mechanical alignment can, therefore, have a significant impact on the variability of the electromagnetic coupling. To deal with this variation, zig–zag geometries [6], shown in Figs. 2 and 3, of both motherboard and memory card flex circuit traces provide coupling strength robustness against residual positional misalignment by stabilizing the overlap area and increasing the relative contribution of fringing fields. Simulations that demonstrate this alignment insensitivity quantitatively are described in Section IV.

During development of the coupler, it was determined that a key feature of the design was that the angular rotation of the conductor segments about the longitudinal axis in conjunction with the number of zig–zag segments could be used to determine the stability of the coupling performance over a given range of X- and Y-axis misalignment. In general terms, larger angular rotations between consecutive conductor segments (angle θ in Fig. 3) were shown to produce greater performance stability in return for a reduction in potential coupling efficiency and directivity. Further, while it is possible to configure both differential signal conductor pairs with corresponding segments parallel or nonparallel, it was established that the nonparallel structure maintains better coupling symmetry in the presence of X- and Y-axis misalignment.

Both the amplitude and width of the coupled pulse determine the energy content of the coupled transmitted signal delivered to the receiving device. The width of the coupled pulse depends on both the rise and fall times of the incident signal and the physical length of the coupled structure. A minimum length coupler design is generally desirable for high circuit density and minimal intersymbol and intrasymbol interference. However, the need to achieve an adequate BER at the receiver without violating transistor performance limitations places a minimum energy transfer constraint on the coupler design. The system design discussed here utilized a full custom differential receiver circuit in an off the shelf 0.25-μm silicon CMOS logic process (described in Section V), and it was determined by simulation that a 1-cm coupler length would provide an adequate level of coupled pulse power at the receiver input. Later analysis of the measured waveforms showed that each coupled load extracted less than 0.1% of the incident signal power in this regime.

The minimum length constraints require the coupler performance to lie between two physical regimes. The coupler must be sufficiently long to provide some distributed line behavior; otherwise it behaves as a lumped capacitance with a corresponding impedance discontinuity. On the other hand, circuit density needs at these data rates and signal frequencies require that it be too short to behave as a traditional quarter-wavelength directional coupler [5]. However, the coupler length must scale (decrease) as frequencies increase to avoid having multiple symbols simultaneously coupling through to the receiver and interfering with each other. This scaling requirement dovetails nicely with the continued need to increase circuit density and integration of digital systems.

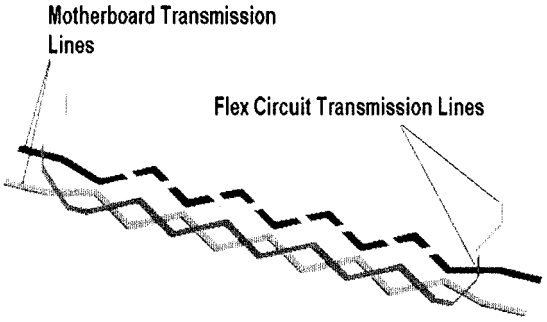

Fig. 2. Coupler zig–zag geometry.

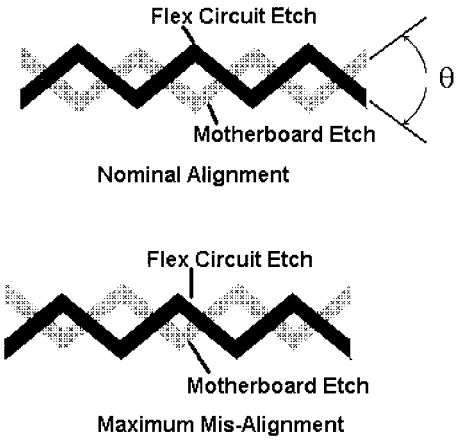

Fig. 3. Alignment of motherboard and flex circuit etches.

The amplitude of the received pulse can be determined by the capacitive and inductive coupling coefficients using the near-end crosstalk coupling coefficient K_{ne} [7]

$$K_{ne} = \frac{1}{4}\left(\frac{C_{12}}{\sqrt{C_{11}C_{22}}} + \frac{L_{12}}{\sqrt{L_{11}L_{22}}}\right) = \frac{1}{4}(K_c + K_l) \quad (1)$$

where C_{12} is the mutual capacitance per unit length between the two coupled traces, C_{11} and C_{22} are the per unit length self-capacitances for the first and second coupled lines, respectively, L_{12} is the mutual inductance per unit length between the two coupled traces, L_{11} and L_{22} are the per unit length self-inductances for the first and second coupled lines, respectively, K_c is the capacitive coupling coefficient, and K_l is the inductive coupling coefficient. Equation (1) strictly applies when the rise time of the incident transmitted signal is less than twice the time of flight across the coupler length $(t_r < 2T_f)$. If this is not true, the near-end coupled amplitude will be reduced.

To estimate the directivity, we also consider the far-end crosstalk coupling coefficient K_{fe} [7]

$$K_{fe} = \frac{1}{2}(K_c - K_l) \quad (2)$$

where K_c and K_l are the capacitive and inductive coupling coefficients as defined above. The ratio between the near-and and far-end coupled voltages is equivalent to the directivity.

III. Coupler Mechanical Design

The mechanical design of couplers for this application was primarily constrained by the accuracy with which the memory card and motherboard conductors can be aligned using large-volume low-cost manufacturing techniques. In the test system, the flex circuit coupled traces broadside couple to the motherboard bus microstrip lines. To implement a separable connector, the coupled traces are microstrip lines on a bent loop of a standard two-metal-layer flex soldered at both ends to the bottom of rigid PC board dual inline memory modules (DIMMs) that carry DRAMs and a buffer chip. The flex circuit was designed using off-the-shelf 0.5- and 4.0-mil-thick polyimide film materials and manufactured using conventional lamination techniques. A socket mounted on the motherboard guides the card and flex assembly down during insertion, pressing the flex loop flat against the motherboard. A vertical pin attached to the bottom of the DIMM passes through holes in the flex and motherboard for alignment of coupled traces to $+/-12$ mil. Figs. 4 and 5 show the dimensions in inches of the motherboard and flex circuit conductors used to form the coupler elements. Fig. 6 shows the flex circuit and motherboard in cross section.

The prototype coupler was fabricated using a two-component connector-type mechanical assembly shown in Fig. 7. A clamping mechanism mounted to the daughter card provides mechanical retention for the ends of the flex circuit and strain relief for the coupler conductors that are flow soldered to contact pads on the daughter card edge. The vertical alignment pin also forms part of this clamp. A second retention structure mounted on the motherboard ensures proper insertion of the daughter

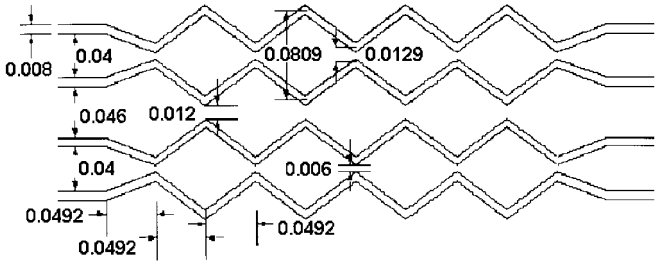

Fig. 4. Motherboard coupler conductor dimensions in inches.

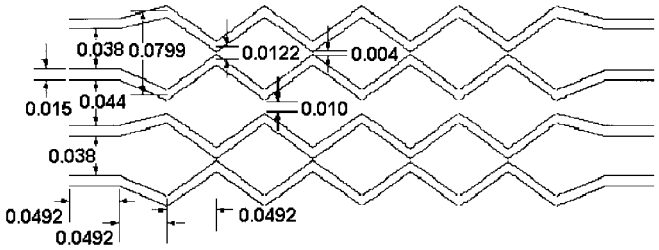

Fig. 5. Flex circuit coupler conductor dimensions in inches.

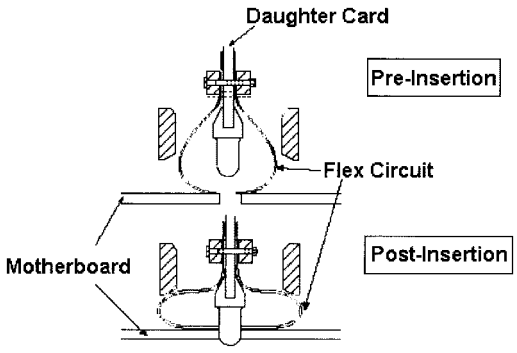

Fig. 6. Coupler–motherboard interface cross section showing the coupler in pre- and post-insertion positions.

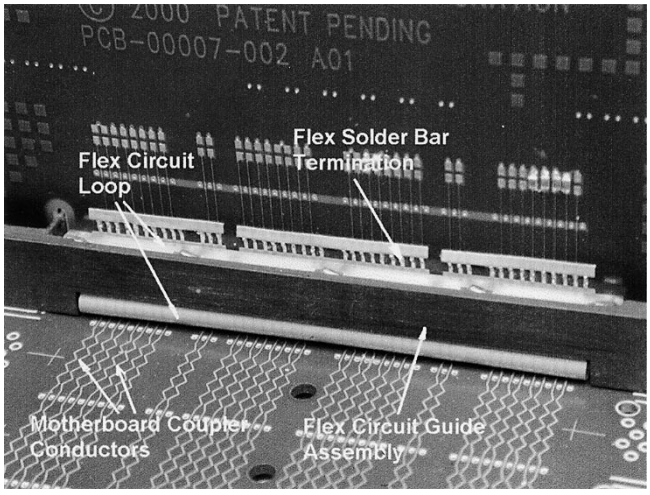

Fig. 7. Coupler in post-insertion position.

card. The test couplers occupy 400 × 42 mil, consistent with the typical DIMM pitch for PC motherboards.

Low-frequency and dc signals like power and ground reach the DIMM card using standard through-hole connections. Metal

TABLE I
MANUFACTURING AND MATERIALS VARIATIONS

Parameter	Nominal	Tolerance
Flex conductor thickness	0.325 mil	± 0.1 mil
Flex conductor width	15 mil	±0.5 mil
Flex substrate thickness	4.0 mil	± 0.1 mil
Flex coverlay thickness	0.5 mil	± 0.1 mil
Soldermask thickness	0.5 mil	± 0.3 mil
Motherboard conductor thickness	1.5 mil	± 0.5 mil
Motherboard conductor width	8 mil	±0.5 mil
Motherboard substrate thickness	5.0 mil	±0.5 mil
FR4 ε_r	4.5	±0.3
Solder Mask ε_r	3.5	±0.3
Polyimide ε_r	3.5	±0.3

pins identical to standard memory connector pins are populated along both sides of the motherboard retention structure so the whole is a hybrid incorporating both ac and dc coupled traces. Preliminary reliability studies, including multiple insertion tests, indicate that the system promises to be robust in volume manufacturing. It can be argued that electromagnetic coupling aids connector reliability since increased conductor separation merely causes less signal energy to appear at the receiver, whereas separation for a directly connected trace creates an open circuit and a catastrophic failure.

IV. SIMULATION AND MODELING

The performance of the coupler was extensively modeled using both Ansoft *Q3D* and Ansoft *HFSS* tools to obtain microwave scattering performance and equivalent electrical parameters. An analysis of the coupler behavior was performed over the anticipated manufacturing spread of dielectric and conductor dimensions and materials properties shown in Table I.

The three-dimensional (3-D) computer model incorporates air gaps resulting from the nonplanarity of the motherboard surface and adhesive squeeze-out in the flex circuit, as shown in the simplified cross section of Fig. 8. The "embossing" of the flex circuit is particularly challenging for maintaining a sufficient coupling coefficient because it both increases the separation between the conductor surfaces in the middle of the flex trace and introduces a low relative dielectric constant over part of the conductor overlap area. Besides altering the flex lamination process to achieve better planarity, the situation can be improved by filling the gaps with a liquid dielectric with a higher dielectric constant. Several such experiments were performed using various household cooking oils and glycerol to confirm the impact of the air gaps. These demonstrated increased coupled voltage, although at the expense of increased impedance

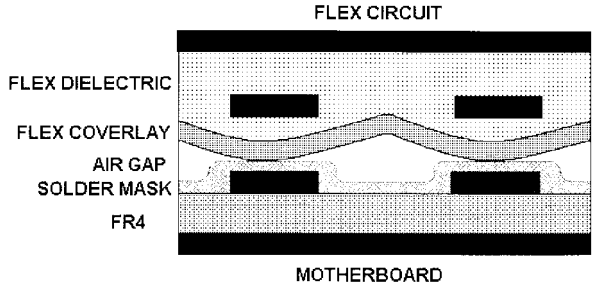

Fig. 8. Simplified coupler cross section showing flex circuit embossing effect.

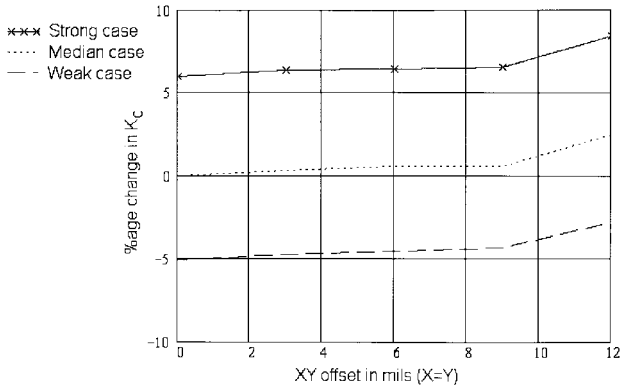

Fig. 9. Percentage K_c variation versus X- and Y-axis offset for strong, median, and weak cases obtained from Ansoft *HFSS* analysis.

mismatch at the coupler inputs in some cases. It is also possible to increase the coupling by simply widening the flex traces, which was done in one of our coupler implementations. Since trace geometries were chosen to provide 50-Ω impedances and the desired coupling in a standard FR4 four-layer PC motherboard stackup, it was necessary to raise the impedance of the flex traces by perforating the ground plane under them. Extensive simulation was used to choose the appropriate density of ground-plane cuts to achieve the desired impedance without adversely impacting overall signal integrity.

In Fig. 9, the variation in the capacitive coupling coefficient due to these variations at nominal alignment (0-mil XY offset) is from approximately $+6\%$ to -5%. The computed variation in K_c with conductor misalignment is also shown for the weakest, median, and strongest coupling scenarios in Fig. 9, and is within 2.5% over 12 mil of X- and Y-axis misalignment. In addition, simulations indicate substantial reduction of K_c variation with vertical offset. For a $+/-30\%$ change in conductor separation, the capacitive coupling coefficient varies by less than $+/-15\%$. For parallel-plate geometries without zig–zags, K_c varies from $+40\%$ to -30% over the same range of conductor separations.

The computed scattering parameters, shown in Fig. 10, demonstrate that the coupling and reflection-coefficient goals were met in the frequency range of interest. Due to the minimal length and mixed-dielectric nature of the coupler, the directivity is approximately 6 dB for the relevant frequencies. Using (1) and (2) with typical values of $K_c = 0.34$ and $K_l = 0.19$, the estimated directivity is 4.9 dB, which is in good agreement with the simulated value.

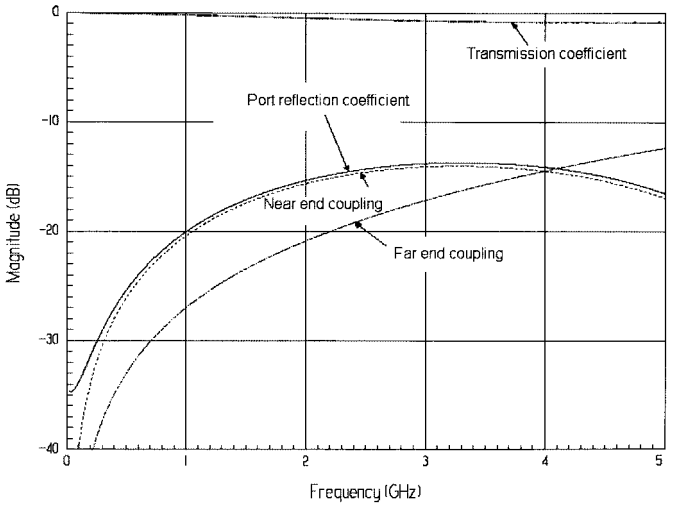

Fig. 10. Computed scattering parameters of 10 MHz–5 GHz.

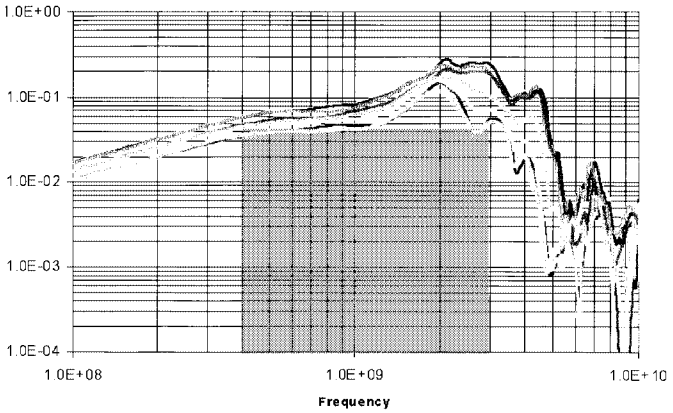

Fig. 11. Simulated channel performance including channel, coupler, and load parameter variations.

V. Receiver Circuit Design

To complete the system, it is necessary to co-design interface circuitry for the memory card buffer chip and the memory controller with the coupler described above. The circuit design can help reduce system cost by providing robust signal reception over a wide range of manufacturing and alignment variations of the coupler, in addition to compensating for on-chip process, supply voltage, and temperature variations. Fig. 11 shows a simulated set of transfer functions from a bus transmitter to a receiver over a variety of system configurations including FR4 dielectric constant and loss coefficient, coupler strength (i.e., magnitude of coupling coefficient), position along the bus, and package parasitics. From this figure, the range of transmitted signal attenuation is between 1/14–1/20, which sets the gain requirement for the receiver amplifier. The shaded region in this figure corresponds to the passband of interest for the transmitted signal, approximately from 400 MHz to 3 GHz. To exploit this constrained bandwidth to achieve ever increasing data rates, it is possible to utilize modulation techniques, but a detailed discussion of this is beyond the scope of this paper. We describe one implementation of pulse-based modulation that balances tradeoffs between spectral efficiency and circuit complexity for high-speed bus applications in [4].

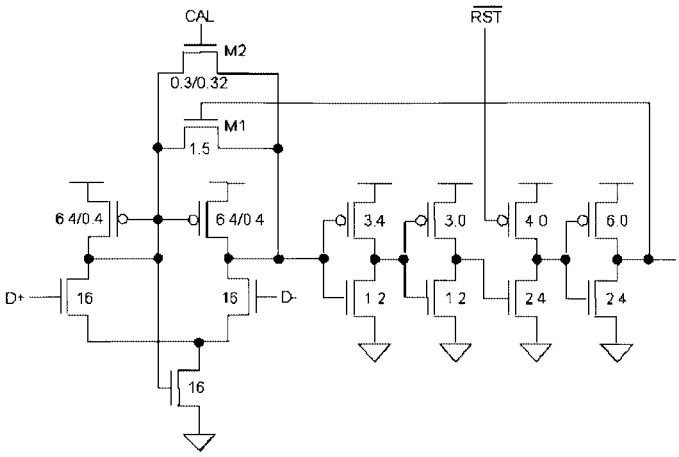

Fig. 12. Differential input receiver.

Fig. 12 shows the integrating amplifier that forms the front end of the interface receiver circuitry. Since the coupler essentially acts as a high-pass filter, it converts each edge of a transmitted pulse into a narrow attenuated received pulse. The receiver amplifies this narrow pulse to rail-to-rail swings and expands its duration for following circuitry. The first stage consists of a self-biased differential amplifier [9] that provides gain and differential to single-ended conversion with additional gain from succeeding inverters. Total gain is approximately 15. While biasing the tail current source device from the current mirror node rather than from a reference current source reduces the power supply rejection ratio (PSRR); the benefits include lower device count, less required voltage headroom, and good tracking between the diff amp output level and the following inverter thresholds over process, voltage, and temperature variations. In addition, almost all of the demodulation circuitry described in [4] depends on matching delays rather than absolute voltage levels so, as long as all circuits see the same power supply variation, the rejection ratio is not critical.

Device $M1$ aids self-reset of the first stage after a pulse has arrived by equalizing the voltage between the bias node and output. $M2$ enables a coarse 1-bit automatic gain control for process, voltage, and temperature variations by providing a resistive connection between the bias and output nodes. The calibration (CAL) signal is derived from the average device speed calibration performed by an integrated digital delay-locked loop (DLL). By using the DLL control codes, it is possible to compute the gain calibration without using an independent feedback loop, thus saving circuit area and complexity. Although this limits the accuracy of the control and does not enable compensation for coupler strength, it is sufficient for the 1.6-Gb/s bus performance.

The final output of the integrating amplifier is a dynamic latch whose precharge is controlled by the reset signal _RST. To implement the self-reset, _RST is fed back from digitally controlled delay elements further down the receive path. Its delay increases, the duration of the received amplified pulses so that less pressure is put on the performance of other circuits responsible for the demodulation [4]. Circuit design was performed in conjunction with coupler design by converting S-parameters and other field solver representations

into primary line parameter matrices that could then be directly incorporated into HSPICE circuit simulations using lossy coupled transmission-line models.

The receiver front end sets a lower bound on both the coupler length and coupling coefficient due to its limited gain-bandwidth product. As the input coupled pulse gets smaller in amplitude or shorter in duration, it is less reliably received, as indicated by the increasing BER. This can be improved, for example, by using a multistage amplifier. However, in parallel bus applications, such as computer memory subsystems, the extra power consumption and latency incurred by additional stages can degrade overall system performance. As the gain-bandwidth product of future CMOS devices increases, it will be possible to use shorter electromagnetic couplers and lower levels of coupled power with single-stage amplifiers as long as BER requirements are met.

VI. Test Results

A set of prototype couplers was fabricated and tested in both the time and frequency domains. Special S-parameter DIMM modules, which incorporated flex circuit couplers, but no buffer chips or DRAMs, were used for coupler characterization. The near end of the couplers was connected to subminiature A (SMA) connectors for interfacing to test equipment. Since the time-domain measurements are most relevant for the receiver circuits, we describe those experimental results below.

For a 1-cm coupler in the FR4/polyimide dielectric system of the installed coupler, the time of flight T_f along the coupler is approximately 70 ps. Typical rise times t_r for transmitted pulses are 240 ps. We expect the coupled pulse duration to be approximately equal to the sum of the rise time and twice the time of flight since the duration of the time-varying incident voltage and current induces a wave that propagates down the length of the coupler and back, and the rise time, in this case, is larger than twice T_f. Thus, the pulse duration should be near 380 ps. Fig. 13 shows a simulated coupled waveform compared to a measured waveform for a pulse propagating on the motherboard trace and received through the coupler at an oscilloscope. Incident signal edges induce coupled pulses of 400-ps width, which is in good agreement with estimated pulsewidth.

After measurement of the coupled signals, the flex circuits were cross sectioned and the dimensions of the laminated layers were measured. The layer thicknesses and conductor widths indicated that the couplers were on the weaker side of the coupling coefficient range. Using (1) with $K_c = 0.27$ and $K_l = 0.14$, an incident differential voltage swing of 2.5 V, and derating by the ratio between twice the time of flight and the rise time (approximately 58%), the estimated peak-to-peak amplitude is 150 mV, which is in excellent agreement with the simulated waveforms in Fig. 10. The measured peak-to-peak voltage is 120 mV. Generally good agreement was achieved between computed and measured coupler performance and waveforms (within 20% in the worst case). The discrepancy is possibly due to impedance mismatches between the SMA connector and

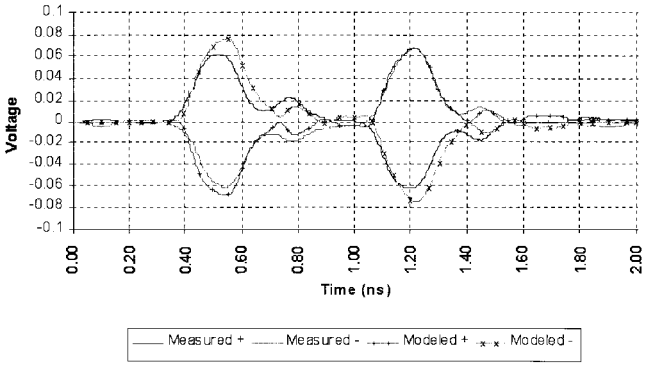

Fig. 13. Computed versus measured differential waveforms.

S-parameter DIMM module trace as the result of a manufacturing error in the S-parameter DIMM. The time-domain simulations were performed using the circuit simulator HSPICE with coupled transmission-line models derived from field simulator data.

After the couplers themselves were characterized, 1.6-Gb/s per differential pair performance was demonstrated in an eight-load prototype memory bus based on the coupler design. The custom I/O transceivers were also tested and characterized by setting input test vectors and acquiring their outputs with a logic analyzer. Multiple memory read and write transactions were executed continuously on the bus for over four weeks without observing a bit error. From these measurements, we estimate that the memory bus BER was less than 2.0e-17.

VII. Summary

Signal integrity continues to be a challenge in high-performance digital systems, especially in low-cost and high-volume applications like PCs. To eliminate the impedance discontinuities and reduce the effects of connector and package parasitics, it is possible to replace direct short-circuit connections with electromagnetically coupled ones. By controlling the coupling coefficients within a desired range that minimizes impedance discontinuities, reflections that contribute to intra-symbol interference and ISI are greatly reduced. A significant challenge is to design a manufacturable coupler that allows end-user configuration while maintaining control over the coupling strength. In this paper, we have described an approach using a zig–zag geometry that reduces the coupling coefficient variation due to misalignment of the coupling elements in all three dimensions. The coupler is implemented using a bent flex loop soldered to a rigid DIMM. Preliminary mechanical testing indicates that the design has potentially high reliability.

We also describe a receiver circuit that can amplify and integrate the attenuated and narrow coupled pulses for further processing by demodulation circuits. While the amplifier gain is currently compensated only for process, voltage, and die temperature variations, it is possible to incorporate compensation for the coupling strength as well. This will continue to reduce cost and enhance reliability by further relaxing the mechanical alignment requirements of the separable coupler. We view this as part of a larger trend in which on-chip circuits compensate for an increasing number of off-chip manufacturing variations.

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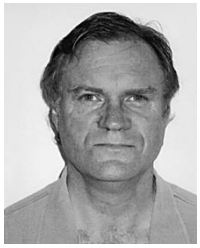

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